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GROUP 2600

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 10/791,945
Filing Date: March 03, 2004
Appellant(s): CHANG ET AL.

Bruce E. Garlick
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/16/2006 appealing from the Office action

mailed 12/19/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

Claims 1, 3-5, 7, 11, 16, 18-20, 22, 26 and 29 were rejected under 35 U.S.C. 102(b) as being anticipated by Pukkila (US 20010017904 A1), these rejection have been withdrawn by the examiner with the purpose to maintain a single rejection for each claim.

Claims 1, 3-5, 7, 11, 16, 18-20, 22, 26 and 29 were rejected twice with two

different references (Pukkila and Parolari), the Examiner will maintain only one of these

rejection for purposes of appeal (Parolari).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20040081248	PAROLARI	4-2004
See NOTE 1		
6909758	RAMESH	6-2005
PCT/EP02/03881	PAROLARI	11-2002
EP1255368	PAROLARI	11-2002

Note 1:   a) Parolari is continuation of PCT/EP02/03881, published in English with

publication number WO 02/091655 on November 14, 2002.

b) Parolari also claims priority of the European patent application

1830283, published as EP 1255368 on November 11, 2002.

For the above reasons, it is believed that the rejections should be sustained.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7, 9-11, 13-22, 24-26 and 28-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Parolari (US 20040081248 A1).

As per claims 1 and 16, Parolari discloses a method for performing Incremental Redundancy (IR) operations in a wireless receiver comprising receiving an analog signal corresponding to a data block (figure 5 antenna paragraph [0112]); sampling the analog signal to produce samples (figure 5 block A/D paragraph [0112]); equalizing the samples to produce soft decision bits of the data block (figure 5 block MLSE paragraph [0112]); configuring, by a system processor of the wireless receiver, a plurality of IR processing module registers (figure 5 block control processor paragraph [0112]); initiating, by the system processor of the wireless receiver, operation of an IR processing module of the wireless receiver (figure 5 block control processor paragraph [0112]); and accessing, by the IR processing module, the plurality of IR processing module registers (figure 5 block control processor paragraph [0112]); and performing, by the IR processing module, IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block (figure 5 block channel decoder and control processor paragraph [0112]).

As per claims 2 and 17, Parolari discloses claims 1 and 16, Parolari also discloses that the data block comprises a complete link layer data-block (figure 5 paragraphs [0011] and [0112]).

As per claims 3 and 18, Parolari discloses claims 1 and 16, Parolari also discloses that the plurality of IR processing module registers comprises the system processor writing the soft decision bits of the data block to the plurality of IR processing module registers (figure 5 control processor paragraph [0112]).

As per claims 4 and 19, Parolari discloses claims 1 and 16, Parolari also discloses that the system processor writing the soft decision bits of the data block to a memory accessible by the IR processing module (figure 5 control processor, channel decoder and redundancy incremental buffer paragraph [0112]).

As per claims 5 and 20, Parolari discloses claims 4 and 19, Parolari also discloses determining that an additional copy of the data block is stored in memory (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); retrieving soft decision bits of the additional copy of the data block (abstract figure 5 control processor paragraphs [0051] and [0061] type II IR); soft combining the soft decision bits of the additional copy of the data block with the soft decision bits of the data block to produce combined soft decision bits of the data block (abstract, paragraphs [0051], [0061], and [0074]; figure 5 paragraphs [0112] and [0113]); and decoding the combined soft decision bits of the data block (figure 5 block channel decoder and IR buffer paragraph [0112]).

As per claims 6 and 21, Parolari discloses claims 5 and 20, Parolari also discloses determining that an additional copy of the data block is stored in memory is based upon type I IR memory contents (paragraph [0051], [0061] and [0074]); and retrieving soft decision bits of the additional copy of the data block includes accessing type II IR memory (paragraph [0051], [0061] and [0074]).

As per claims 7 and 22, Parolari discloses claims 5 and 20, Parolari also discloses the IR processing module identifying an IR mode of the additional copy of the data block stored in memory (paragraph [0051]).

As per claims 9 and 24, Parolari discloses claims 5 and 20, Parolari also discloses assigning different weights to each of the data block and the additional copy of the data block for soft combining (abstract, paragraph [0073], [0143], [0144], [0154], [0156], [0175] and [0182]).

As per claims 10 and 25, Parolari discloses claims 9 and 24, Parolari also discloses that the weights are assigned to the data block and to the additional copy of the data block based upon respective measured signal qualities ([0073], [0074] and [0076]).

As per claims 11 and 26, Parolari discloses claims 5 and 20, Parolari also discloses storing the combined soft decision bits of the data block in memory for later use ([0073] and [0074]).

As per claims 13 and 28, Parolari discloses claims 1 and 16, Parolari also discloses storing the soft decision bits of the data block in IR memory (figure 5 paragraph [0112]).

As per claims 14 and 30, Parolari discloses claims 1 and 16, Parolari also discloses failing to correctly decode a header of the data block (figure 5 paragraph [0112] and [0163]); and discarding the soft decision bits of the data block (figure 5 paragraph [0112] and [0163]).

As per claims 15 and 31, Parolari discloses claims 1 and 16, Parolari also discloses each symbol of the data block is represented by four punctured soft decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits (paragraph [0074] and tables 1-4).

As per claim 29, Parolari discloses claim 16, Parolari also discloses that the system processor is further operable to store the soft decision bits of the data block in an IR memory (figure 5 paragraph [0112]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 12, 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parolari as applied to claims 1 and 16 above, and further in view of Ramesh (US 6909758 B2).

As per claims 8 and 23, Parolari discloses claims 7 and 22, Parolari also discloses identifying a puncturing pattern of the additional copy of the data block stored in memory (paragraph [0074]). Parolari doesn't specifically disclose the inherently

depuncturing process of depuncturing the copy of the data block stored in memory

when required (paragraph [0074]). Ramesh discloses depuncturing the copy of the data

block stored in memory (figure 2 block 240 column 5 lines 41-51 and figure 5 block 510

column 7 lines 21-32). Parolari and Ramesh are analogous art because they are from

the same field of endeavor. At the time of the invention, it would have been obvious to a

person of ordinary skill in the art to incorporate the decoding technique disclosed by

Ramesh in the link adaptation process disclosed by Parolari. The suggestion/motivation

for doing so would have been to depuncturing a punctured data block (Ramesh column

4 lines 30-34).

     As per claims 12 and 27, Parolari discloses claims 1 and 16, Parolari also

discloses decoding the soft decision bits of the data block to produce a decoded header

(figures 4-5 channel decoder paragraphs [0024]-[0026] and [0074]); and identifying a

Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block

from the decoded header (paragraphs [0074]-[0079]). Parolari doesn't specifically

disclose the inherently depuncturing process, depuncturing the soft decision bits of the

data block based upon the MCS mode and puncturing pattern to produce depunctured

soft decision bits; and decoding the depunctured soft decision bits. Ramesh discloses

depuncturing the soft decision bits of the data block based upon the MCS mode and

puncturing pattern to produce depunctured soft decision bits (figure 2 block 240 column

5 lines 41-51 and figure 5 block 510 column 7 lines 21-32); and decoding the

depunctured soft decision bits (figure 2 block 240 column 4 lines 22-34 and figure 5

block 580 column 8 lines 23-36). Parolari and Ramesh are analogous art because they

are from the same field of endeavor. At the time of the invention, it would have been

obvious to a person of ordinary skill in the art to incorporate the decoding technique

disclosed by Ramesh in the link adaptation process disclosed by Parolari. The

suggestion/motivation for doing so would have been to depuncturing a punctured data

block (Ramesh column 4 lines 30-34).

Double Patenting

Claims 1, 12, 27, 16, 1, 12, and 31 of this application, conflict with claims 1, 6, 7,

14, 27, 28 and 34 respectively of Application No. 10/731,803. 37 CFR 1.78(b) provides

that when two or more applications filed by the same applicant contain conflicting

claims, elimination of such claims from all but one application may be required in the

absence of good and sufficient reason for their retention during pendency in more than

one application. Applicant is required to either cancel the conflicting claims from all but

one application or maintain a clear line of demarcation between the applications. See

MPEP § 822.

The nonstatutory double patenting rejection is based on a judicially created

doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent

and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11

F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225

USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA

1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*,

418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be

used to overcome an actual or provisional rejection based on a nonstatutory double

patenting ground provided the conflicting application or patent is shown to be commonly

owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a

terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with

37 CFR 3.73(b).

Claims 1, 12, 27, 16, 1, 12, and 31 are provisionally rejected under the judicially

created doctrine of obviousness-type double patenting as being unpatentable over

claims 1, 6, 7, 14, 27, 28 and 34 respectively of copending Application No. 10/731,803.

Although the conflicting claims are not identical, they are not patentably distinct from

each other because claims are substantially the same.

As per claims 1 (10/731803) and 1 (10/791945) application with serial No.

10/731803 claims "A system for implementing Incremental Redundancy (IR) operations

in a wireless receiver comprising: a baseband processor that is operable to receive

analog signals corresponding to a data block and to sample the analog signal to

produce samples; an equalizer that is operable to receive the samples from the

baseband processor, to equalize the samples, and to produce soft decision bits of the

data block; a system processor that is operable to receive the soft decision bits and to

initiate IR operations; and an IR processing module operably coupled to the system

processor that is operable to receive the soft decision bits and to perform IR operations

on the soft decision bits" and application with serial No. 10/791945 claims "A method for

performing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving an analog signal corresponding to a data block; sampling the analog signal to

produce samples; equalizing the samples to produce soft decision bits of the data block;

configuring, by a system processor of the wireless receiver, a plurality of IR processing

module registers; initiating, by the system processor of the wireless receiver, operation

of an IR processing module of the wireless receiver; and accessing, by the IR

processing module, the plurality of IR processing module registers; and performing, by

the IR processing module, IR operations on the soft decision bits of the data block in an

attempt to correctly decode the data block". 10/731803 and 10/791945 are analogous

art because they are from the same field of endeavor. At the time of the invention, it

would have been obvious to a person of ordinary skill in the art to incorporate

initialization and accessing disclosed by 10/791945 to processing disclosed by

10/731803. The suggestion/motivation for doing so would have been that processing

inherently includes initialization and accessing.

As per claim 6 (10/731803) and 12 (10/791945), application with serial No.

10/731803 claims "the soft decision bits of the data block are stored in IR memory; a

determination is made that a Modulation and Coding Scheme (MCS) mode and

puncturing pattern of the subsequently received copy of the data block and a MCS

mode of the data block are compatible; soft decision bits of the subsequently received

copy of the data block are combined with soft decision bits of the data block to produce

combined soft decision bits; the combined soft decision bits are depunctured; and the IR

processing module decodes the depunctured combined soft decision bits" and

application with serial No. 10/791945 claims "decoding the soft decision bits of the data

block to produce a decoded header; and identifying a Modulation and Coding Scheme

(MCS) mode and puncturing pattern of the data block from the decoded header;

depuncturing the soft decision bits of the data block based upon the MCS mode and

puncturing pattern to produce depunctured soft decision bits; and decoding the

depunctured soft decision bits". 10/731803 and 10/791945 are analogous art because

they are from the same field of endeavor. At the time of the invention, it would have

been obvious to a person of ordinary skill in the art to incorporate initialization and

accessing disclosed by 10/791945 to processing disclosed by 10/731803. The

suggestion/motivation for doing so would have been that processing inherently includes

initialization and accessing.

As per claims 7 (10/731803) and 27 (10/791945), application with serial No.

10/731803 claims "a determination is made that a Modulation and Coding Scheme

(MCS) mode of the subsequently received copy of the data block and a MCS mode and

puncturing pattern of the data block are compatible; the soft decision bits of the data

block are depunctured to produce first depunctured soft decision bits; the soft decision

bits of data of the subsequently received copy of the data block are depunctured to

produce second depunctured soft decision bits; the first depunctured soft decision bits

and the second depunctured soft decision bits are combined to produce combined

depunctured soft decision bits; and the IR processing module is operable to decode the

combined depunctured soft decision bits." and application with serial No. 10/791945

claims "decode the soft decision bits of the data block to produce a decoded header;

and identify a Modulation and Coding Scheme (MCS) mode and puncturing pattern of

the data block from the decoded header; depuncture the soft decision bits of the data

block based upon the MCS mode and puncturing pattern to produce depunctured soft

decision bits; and decode the depunctured soft decision bits". 10/731803 and

10/791945 are analogous art because they are from the same field of endeavor. At the

time of the invention, it would have been obvious to a person of ordinary skill in the art

to incorporate initialization and accessing disclosed by 10/791945 to processing

disclosed by 10/731803. The suggestion/motivation for doing so would have been that

processing inherently includes initialization and accessing.

As per claims 14 (10/731803) and 16 (10/791945), application with serial No.

10/731803 claims "A system for implementing Incremental Redundancy (IR) operations

in a wireless receiver comprising: at least one processing device that is operable to

receive an analog signal corresponding to a data block, to sample the analog signal to

produce samples, to equalize the samples, to produce soft decision bits of the data

block, and to initiate IR operations; and an IR processing module operably coupled to

the at least one processing device that is operable to receive the soft decision bits and

to perform IR operations on the soft decision bits" and application with serial No.

10/791945 claims "A system for implementing Incremental Redundancy (IR) operations

in a wireless receiver comprising: a baseband processor that is operable to receive

analog signals corresponding to a data block and to produce samples of the analog

signals; an equalizer that is operable to receive the samples from the baseband

processor, to equalize the samples, and to produce soft decision bits of the data block;

a system processor that is operable to receive the soft decision bits of the data block; a

plurality of IR processing module registers communicatively coupled to the system

processor; an IR processing module communicatively coupled to the system processor

and to the plurality of IR processing module registers; wherein the system processor is

operable to configure the plurality of IR processing module registers and to initiate

operation of the IR processing module of the wireless receiver; and wherein the IR

processing module is operable to access the plurality of IR processing module registers,

to receive the soft decision bits of the data block, and to perform IR operations on the

soft decision bits of the data block in an attempt to correctly decode the data block".

10/731803 and 10/791945 are analogous art because they are from the same field of

endeavor. At the time of the invention, it would have been obvious to a person of

ordinary skill in the art to incorporate initialization and accessing disclosed by

10/791945 to processing disclosed by 10/731803. The suggestion/motivation for doing

so would have been that processing inherently includes initialization and accessing.

As per claims 27 (10/731803) and 1 (10/791945) application with serial No.

10/731803 claims "A method for performing Incremental Redundancy (IR) operations in

a wireless receiver comprising: receiving an analog signal corresponding to a data

block; sampling the analog signal to produce samples; equalizing the samples to

produce soft decision bits of the data block; transferring the soft decisions of the data

block to an IR processing module; and the IR processing module receiving the soft

decision bits of the data block and performing IR operations on the soft decision bits of

the data block in an attempt to correctly decode the data block" and application with

serial No. 10/791945 claims "A method for performing Incremental Redundancy (IR)

operations in a wireless receiver comprising: receiving an analog signal corresponding

to a data block; sampling the analog signal to produce samples; equalizing the samples

to produce soft decision bits of the data block; configuring, by a system processor of the

wireless receiver, a plurality of IR processing module registers; initiating, by the system

processor of the wireless receiver, operation of an IR processing module of the wireless

receiver; and accessing, by the IR processing module, the plurality of IR processing

module registers; and performing, by the IR processing module, IR operations on the

soft decision bits of the data block in an attempt to correctly decode the data block".

10/731803 and 10/791945 are analogous art because they are from the same field of

endeavor. At the time of the invention, it would have been obvious to a person of

ordinary skill in the art to incorporate initialization and accessing disclosed by

10/791945 to processing disclosed by 10/731803. The suggestion/motivation for doing

so would have been that processing inherently includes initialization and accessing.

As per claims 28 (10/731803) and 12 (10/791945) application with serial No.

10/731803 claims "decoding the soft decision bits of the data block to produce a

decoded header; and determining a Modulation and Coding Scheme (MCS) mode and

puncturing pattern of the data block from the decoded header; depuncturing the soft

decision bits of the data block based upon the MCS mode and puncturing pattern to

produce depunctured soft decision bits; and the IR processing module decoding the

depunctured soft decision bits" and application with serial No. 10/791945 claims

"decoding the soft decision bits of the data block to produce a decoded header; and

identifying a Modulation and Coding Scheme (MCS) mode and puncturing pattern of the data block from the decoded header; depuncturing the soft decision bits of the data block based upon the MCS mode and puncturing pattern to produce depunctured soft decision bits; and decoding the depunctured soft decision bits". 10/731803 and 10/791945 are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate initialization and accessing disclosed by 10/791945 to processing disclosed by 10/731803. The suggestion/motivation for doing so would have been that processing inherently includes initialization and accessing.

As per claims 34 (10/731803) and 31 (10/791945) application with serial No. 10/731803 claims "each symbol of the data block is represented by four punctured soft decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits" and application with serial No. 10/791945 claims "each symbol of the data block is represented by four punctured soft decision bits; and each symbol of the data block is also represented by five depunctured soft decision bits". 10/731803 and 10/791945 are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate initialization and accessing disclosed by 10/791945 to processing disclosed by 10/731803. The suggestion/motivation for doing so would have been that processing inherently includes initialization and accessing.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

(10) Response to Argument

Applicant's arguments filed on 10/16/2006 have been fully considered but they

are not persuasive.

<u>Regarding claim 1 anticipated by Parolari:</u>

The Applicant contends, "Applicants concede that Parolari fairly discloses the

elements of (a) receiving, (b) sampling, and (c) equalizing of claim 1. Applicants urge

that Parolari fails to disclose, suggest, or teach the elements of (d) configuring, (e)

initiating, (f) accessing, or (g) performing of claim 1. In asserting that Parolari meets all

elements (d)-(g) of claim 1, the Office Action cites the block control processor of FIG. 5

described at paragraph [0112] of Parolari as disclosing elements (d), (e), (f), and (g) of

claim 1. The Office Action also cites the block channel decoder of FIG. 5 in meeting

element (g) of claim 1. Parolari describes at paragraph [0112] (page 11 bottom portion

of column): "Incremental redundancy strategy supported by an Incremental Redundancy

buffer for temporarily storing RLC blocks to be retransmitted under ARQ. A buffer

overflow activates a signal IRout directed to the Control Processor. Decoded RLC

signaling blocks, indicated with DATA- EXTR, are extracted and sent to the Control

Processor for the correct interpretation and execution (such as: Power control, Timing

Advance, Handover, etc.). At best, Parolari describes generally how a control processor

oversees/controls IR processing and how RLC blocks may be stored in an IR buffer for

retransmission, not storage of received punctured data blocks. Parolari further

describes in its later portions IR processes that may be implemented for link adaptation

purposes. However, these details do not disclose any other structure that performs IR

processing of received punctured data. Stated simply, Parolari fails to disclose either an

IR processing module or IR processing module registers as illustrated in FIG. 5B of the

present application. The Office Action equates FIG. 5 block control processor paragraph

[0112] of Parolari with (d) "configuring, by a system processor of the wireless receiver, a

plurality of IR processing module registers" of claim 1. As described above, these

portions of Parolari described generally some aspects of an IR process. These and

other portions of Parolari do not disclose, suggest, or teach (d) "configuring, by a

system processor of the wireless receiver, a plurality of IR processing module registers"

as required by claim 1. The Office Action equates FIG. 5 block control processor

paragraph [0112] of Parolari with (e) "initiating, by the system processor of the wireless

receiver, operation of an IR processing module of the wireless receiver" of claim 1. As

described above, these portions of Parolari described generally some aspects of an IR

process. These and other portions of Parolari do not disclose, suggest, or teach (e)

"initiating, by the system processor of the wireless receiver, operation of an IR

processing module of the wireless receiver" as required by claim 1. The Office Action

equates FIG. 5 block control processor paragraph [0112] of Parolari with (f) "accessing,

by the IR processing module, the plurality of IR processing module registers" of claim 1.

As described above, these portions of Parolari described generally some aspects of an

IR process. These and other portions of Parolari do not disclose, suggest, or teach (f)

"accessing, by the IR processing module, the plurality of IR processing module

registers" as required by claim 1. The Office Action equates FIG. 5 block channel

decoder and control processor paragraph [0112] of Parolari with (g) "performing, by the

IR processing module, IRoperations on the soft decision bits of the data block in an

attempt to eon'eetly decode the data block." As described above, these portions of

Parolari described generally some aspects of an IR process. These and other portions

of Parolari do not disclose, suggest, or teach (g) "performing, by the IR processing

module, IR operations on the soft decision bits of the data block in an attempt to

correctly decode the data block" of claim 1".

The Examiner disagrees and asserts, that, as indicated in the previous Office

action, Parolari discloses accessing, by the IR processing module, the plurality of IR

processing module registers (figure 5 block control processor paragraph [0112]); and

performing, by the IR processing module, IR operations on the soft decision bits of the

data block in an attempt to correctly decode the data block (figure 5 block channel

decoder and control processor paragraph [0112]). Specifically Parolari discloses in:

a) paragraph [0051] that "In EGPRS TBF the transfer of RLC Data Blocks in the

acknowledged RLC/MAC mode can be controlled by a selective type I ARQ

mechanism, or by type II hybrid ARQ mechanism dealing with Incremental Redundancy

(IR), both coupled with the numbering of the RLC Data Blocks within one Temporary

Block Flow. In the type I ARQ mode, decoding of an RLC Data Block is solely based on

the prevailing transmission (i.e. erroneous blocks are not stored). In the type II hybrid

ARQ case, **erroneous blocks are stored by the receiver and a joint decoding with**

new transmissions concerning original blocks is done. If the memory for IR

operation run out in the MS, the MS shall indicate this by setting an LA/IR bit in the

EGPRS PACKET DOWNLINK ACK/NACK message. Type II hybrid ARQ is mandatory

in EGPRS MS receivers" (emphasis added);

    b) paragraph [0061] Parolari also discloses "Incremental redundancy pertaining

to type II hybrid ARQ, differently from type I ARQ, needs a lot of memory to store

erroneous block together with multi-bits soft decisions usable in joint decoding the

successive retransmitted bits" (emphasis added);

    c) paragraph [0074] Parolari also discloses "Furthermore, it is mandatory for an

.EGPRS MS receiver to be able to perform joint decoding among blocks with different

MCSs if the combination of MCSs is one of the following: MCS-5 and MCS-7; MCS-6

and MCS-9";

    d) paragraph [0112] Parolari discloses that "More precision is obtained delaying

the decision of the MLSE estimator until the end of the burst. At the output of the MLSE

estimator a copy of the original burst is reproduced and each bit is accompanied with

three bits soft decisions indicating its received level. The estimated burst is delivered to

a cascade of the following blocks: Burst disassembler, Deciphering, De-interleave, and

Channel decoder; the last carries out the specified operations in respect of TABLES 1

and 2 by exploiting soft decisions. Control Processor generates the following two

signals: MOD-RX-SEL and CPS-RX-SEL towards MLSE estimator and Channel

decoder respectively. That because modulation and/or code scheme of the received

signal can differ from the transmitted ones. MLSE estimator operates with either GMSK

or 8-PSK modulation, obviously with different trellis and branch metric expression.

Channel decoder uses Soft decisions to carry out convolutional decoding and also takes

advantage from the mentioned Incremental redundancy strategy supported by an

Incremental Redundancy buffer for temporarily storing RLC blocks to be retransmitted

under ARQ";

e) paragraph [0117] Parolari also discloses "means allocated both to the BTS

and the mobile stations for decoding RLC received blocks, optionally capable of joint

decoding Incremental Redundancy bits" (emphasis added) and;

f) finally in the original filed application Parolari claims in claim 5 "temporarily

storing errored data blocks in a memory buffer for joint decoding them with new

transmissions of original blocks according to the incremental redundancy technique".

For these reasons and the reasons indicated in the previous Office action the

rejection of claim 16 is maintained.

Regarding claims 3-5, 7 and 11 anticipated by Parolari:

The Applicant contends, "Parolari fails to anticipate claim 1 for any and all of the

reasons provided above. Because claims 3-5, 7, and 11 depend from claim 1, Parolari

fails to anticipate claims 3-5, 7, and 11 for these Same reasons. Claims 3-5, 7, and 11

require additional operations by/with the IR processing module and/or the plurality of IR

processing module registers. Parolari fails to disclose the IR processing module and the

plurality of processing module registers. Thus, Parolari fails to anticipate claims 3-5, 7,

and 11 for these additional reasons".

The Examiner disagrees and asserts, that, as indicated in the previous Office

action, because the rejection of claim 1 is maintained, the rejections of claims 3-5, 7 and

11 are also maintained.

Regarding claim 16 anticipated by Parolari:

The Applicant contends, "Independent claim 16 is directed to a "system for

implementing Incremental Redundancy (IR) operations in a wireless receiver." The

elements of claim 16 include: (a) a baseband processor that is operable to receive

analog signals corresponding to a data block and to produce samples of the analog

signals; (b) an equalizer that is operable to receive the samples from the baseband

processor, to equalize the samples, and to produce soft decision bits of the data block;

and (c) a system processor that is operable to receive the soft decision bits of the data

block. These elements and their recited functions are fairly taught by Parolari. The other

elements of claim 16 are not fairly taught by Parolari. Claim 16 further requires: (d) a

plurality of IR processing module registers communicatively coupled to the system

processor; and (e) an IR processing module communicatively coupled to the system

processor and to the plurality of IR processing module registers; (f) wherein the system

processor is operable to configure the plurality of IR processing module registers and to

initiate operation of the IR processing module of the wireless receiver; and (g) wherein

the IR processing module is operable to access the plurality of IR processing module

registers, to receive the soft decision bits of the data block, and to perform IR operations

on the soft decision bits of the data block in an attempt to correctly decode the data

block. The Office Action cites the block control processor of FIG. 5 described at

paragraph [0112] of Parolari as disclosing elements (d), (e), (f), and (g) of claim 16. The

Office Action also cites the block channel decoder of FIG. 5 in meeting element (g) of

claim 16. However, Parolari fails to disclose either an IR processing module or IR

processing module registers, which are required by elements (d)-(g) of claim 16. For

these reasons, Parolari fails to anticipate claim 16".

The Examiner disagrees and asserts, that, as indicated in the previous Office

action, Parolari discloses accessing, by the IR processing module, the plurality of IR

processing module registers (figure 5 block control processor paragraph [0112]); and

performing, by the IR processing module, IR operations on the soft decision bits of the

data block in an attempt to correctly decode the data block (figure 5 block channel

decoder and control processor paragraph [0112]). Specifically Parolari discloses in:

a) paragraph [0051] that "In EGPRS TBF the transfer of RLC Data Blocks in the

acknowledged RLC/MAC mode can be controlled by a selective type I ARQ

mechanism, or by type II hybrid ARQ mechanism dealing with Incremental Redundancy

(IR), both coupled with the numbering of the RLC Data Blocks within one Temporary

Block Flow. In the type I ARQ mode, decoding of an RLC Data Block is solely based on

the prevailing transmission (i.e. erroneous blocks are not stored). In the type II hybrid

ARQ case, erroneous blocks are stored by the receiver and a joint decoding with new

transmissions concerning original blocks is done. If the memory for IR operation run out

in the MS, the MS shall indicate this by setting an LA/IR bit in the EGPRS PACKET

DOWNLINK ACK/NACK message. Type II hybrid ARQ is mandatory in EGPRS MS

receivers" (emphasis added);

b) paragraph [0061] Parolari also discloses "Incremental redundancy pertaining

to type II hybrid ARQ, differently from type I ARQ, needs a lot of memory to store

erroneous block together with multi-bits soft decisions <u>usable in joint decoding</u> the

successive retransmitted bits" (emphasis added);

c) paragraph [0074] Parolari also discloses "Furthermore, it is mandatory for an

EGPRS MS receiver to be able to perform <u>joint decoding among blocks with different</u>

<u>MCSs</u> if the combination of MCSs is one of the following: MCS-5 and MCS-7; MCS-6

and MCS-9";

d) paragraph [0112] Parolari discloses that "More precision is obtained delaying

the decision of the MLSE estimator until the end of the burst. <u>At the output of the MLSE</u>

<u>estimator a copy of the original burst is reproduced and each bit is accompanied with</u>

<u>three bits soft decisions indicating its received level</u>. The estimated burst is delivered to

a cascade of the following blocks: Burst disassembler, Deciphering, De-interleave, and

Channel decoder; the last carries out the specified operations in respect of TABLES 1

and 2 by exploiting <u>soft decisions</u>. Control Processor generates the following two

signals: MOD-RX-SEL and CPS-RX-SEL towards MLSE estimator and Channel

decoder respectively. That because modulation and/or code scheme of the received

signal can differ from the transmitted ones. <u>MLSE estimator operates with either GMSK</u>

<u>or 8-PSK modulation, obviously with different trellis and branch metric expression.</u>

<u>Channel decoder uses Soft decisions to carry out convolutional decoding and also takes</u>

<u>advantage from the mentioned Incremental redundancy strategy</u> supported by an

Incremental Redundancy buffer for temporarily storing RLC blocks to be retransmitted

under ARQ";

e) paragraph [0117] Parolari also discloses "means allocated both to the BTS

and the mobile stations <u>for decoding RLC received blocks, optionally capable of joint</u>

<u>decoding Incremental Redundancy bits</u>" (emphasis added) and;

f) finally in the original filed application Parolari claims in claim 5 "<u>temporarily</u>

<u>storing errored data blocks in a memory buffer for joint decoding them with new</u>

<u>transmissions of original blocks according to the incremental redundancy technique</u>".

For these reasons and the reasons indicated in the previous Office action the

rejection of claim 16 is maintained.

<u>Regarding claims 18-20, 22, 26 and 29 anticipated by Parolari:</u>

The Applicant contends, "Claims 18-20, 22, 26, and 29 depend from claim 16.

Parolari fails to anticipate these claims for at least the reasons described above with

respect to claim 16. Claims 18-20, 22, 26, and 29 require additional operations by/with

the IR processing module and/or the plurality of IR processing module registers.

Parolari fails to disclose the IR processing module and the plurality of processing

module registers. Thus, Parolari fails to anticipate claims 18-20, 22, 26, and 29 for these

additional reasons".

The Examiner disagrees and asserts, that, as indicated in the previous Office

action, because the rejection of claim 16 is maintained, the rejections of claims 18-20,

22, 26, and 29 are also maintained.

<u>Regarding claims 8, 12, 23 and 27 anticipated by Parolari in view of Ramesh:</u>

The Applicant contends, "For the reasons provided above with reference to

claims 1 and 16, Parolari fails to meet all of the elements of claims 1 and 16. Ramesh is

cited for its teachings relating to depuncturing of punctured data blocks stored in memory. Ramesh fails to meet the shortcomings of Parolari. For these reasons, the combination of Parolari and Ramesh does not meet the limitations of claims 1 and 16. Claims 8 and 12 and claims 23 and 27 depend from claims 1 and 16, respectively. Thus, for the reasons provided above with respect to claims 1 and 16, the combination of Parolari and Ramesh fails to render obvious claims 8, 12, 23, and 27".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, because the rejection of claims 1 and 16 are maintained, the rejections of claims 8, 12, 23 and 27 are also maintained.
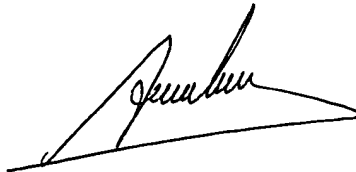
(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

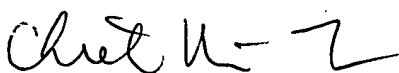Respectfully submitted,

Juan Alberto Torres

11-01-2006

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